Cancel claims 21, 22, 24-29.

Claim 23, line 1, change "21" to --34--;

Claim 30, line 1, change "21" to --34--;

Claim 31, line 1, change "21" to --34--;

Claim 32, line 1, change "21" to --34--;

Claim 33, line 1, change "21" to --34--;

Add new claims 34-39:

--34. A recessed gate field effect power MOS device having a vertically oriented channel comprising:

a semiconductor substrate including first and second laterally-extending layers of first and second opposite polarity dopants defining a body layer and an underlying drain layer;

a first trench having sidewalls extending depthwise from an upper surface of the substrate at least through the body layer to a bottom wall at a predetermined depth from the upper surface of the substrate;

a gate oxide layer on the first trench sidewalls and bottom wall;

a gate conductor filling the first trench depthwise to at least an elevation of the upper surface of the substrate and contacting the gate oxide layer on the trench sidewalls;

a second trench having sidewalls extending depthwise from the upper surface of the substrate to a bottom wall at a second predetermined depth in the body layer spaced above the drain layer, the first trench and the second trench being spaced apart by a predetermined lateral distance;

a vertically oriented [layer] of semiconductor substrate laterally positioned between the first trench and the second trench extending upward along the gate oxide layer from the body layer to the upper surface of the substrate; and

a vertically-extending source conductor contacting the bottom wall and sidewalls of the second trench including contacting [the vertically oriented layers] on both sides of the second trench and opposite the gate oxide layer and gate conductor and contacting the laterally-extending body layer along the bottom wall;

the vertically-oriented layer including a first vertical layer portion contiguous with the body layer doped with said first polarity dopant and a second vertical layer portion atop the first vertical layer portion and doped with [a] said second polarity dopant to form a PN junction with the first vertical layer portion;

the first vertical layer portion being doped with said first polarity dopant to a first doping concentration to define an active body region, including a vertical channel having a threshold characteristic determined by the first doping concentration;

the second vertical layer portion being doped with said second polarity dopant to form a source region contacting the active body region;

the source conductor electrically shorting the source region to the active body region across the PN junction; and

a top portion of the body layer extending horizontally and confined to the bottom of the second trench, spaced depthwise along the trench sidewalls below [the PN junctions], in contact with the source conductor along the bottom wall, being doped to a second doping concentration contained within the body layer, the second doping concentration being greater than the first doping concentration and sufficient to reduce pinched base resistance and thereby prevent parasitic bipolar turnon in the presence of avalanche current, independent of the threshold characteristic of the vertical channel in the active body region.--

--35. A recessed gate field effect power MOS device according to claim 34 including a vertically-oriented insulative layer extending upward from the upper surface of the substrate atop the vertically oriented layer.--

--36. A recessed gate field effect power MOS device according to claim 35 including one of said vertically-oriented layers on each side of the trench, each having one of said vertically-oriented insulative layers thereon, and an insulative layer extending laterally between the sidewall spacers over the gate conductor.--

--37. A recessed gate field effect power MOS device according to claim 35 in which the vertically oriented layer and the gate oxide layer have a combined lateral thickness less than a lateral thickness of the vertically-oriented insulative layer.--

--38. A recessed gate field effect power MOS device according to claim 37 in which the lateral thickness of the vertically-oriented insulative layer is in a range of 0.5 to 1.0 micrometer.--

--39. A recessed gate field effect power MOS device according to claim 34 in which the vertically-oriented layer has a lateral thickness of less than 0.5 micron.--

REMARKS

Claims 21-33 are pending in the application. Claims 21, 22, 24-29 are canceled. New claims 34-39 have been added. Claims 23, 30-33 are amended to depend from claim 34. Claims 23; 30-39 remain in the application. The pending claims should be allowable over the art of record in the prior application.

The application is amended to correct typographical errors.

Enclosed are formal drawings incorporating changes to FIGS. 11-12, 18-19 and 20-21, made in the parent application. The correction to FIG. 11 is to conform to the specification at page 13, lines 10-13, and the change to FIGS. 19-20 conforms to page 13, lines 4-5.